16.265 Logic Design Laboratory Grade Sheet

This page should be stapled together with the rest of the report. After the grading, this page will be taken and kept by the TAs for the record.

1. (This section to be completed by student)

Student logic number: 117

Student name: (Last) \_\_\_\_E\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, (first) \_\_\_\_\_\_\_Erdun\_\_\_\_\_\_\_\_\_\_\_\_\_

Experiment number: 3

Date/time: \_\_04\_\_\_\_/\_\_\_04\_\_/ \_\_\_\_2018\_\_\_, \_\_\_\_\_\_1\_\_\_\_p.m.

1. Preliminary checking
2. Is the report written on 8½” x 11” paper and stapled at left margin?
3. Is a cover page included?
4. Is the report written using the given template?
5. Is the correct assignment used in design?

Report will not be accepted if the answer is “NO” to any of the above questions.

1. Grade

1. Design procedures: supporting theory, details, etc. (20) \_\_\_\_\_\_\_\_\_\_\_

23. Is design correct? (60) \_\_\_\_\_\_\_\_\_\_\_

3. Minimization of design (10) \_\_\_\_\_\_\_\_\_\_\_

5. List of ICs and unused gates (10) \_\_\_\_\_\_\_\_\_\_\_

Gross grade (100) \_\_\_\_\_\_\_\_\_\_

1. Adjustment to grade

1. Grade sheet, cover page (5) \_\_\_\_\_\_\_\_\_\_\_

2. Title box of schematic diagram (5) \_\_\_\_\_\_\_\_\_\_\_

3. Schematic diagram in correct format (10) \_\_\_\_\_\_\_\_\_\_\_

4. Misrepresentation of test (simulation) results (30) \_\_\_\_\_\_\_\_\_\_\_

1. 5. Neatness and legibility (10) \_\_\_\_\_\_\_\_\_\_
2. 6. Templates (20) \_\_\_\_\_\_\_\_\_\_

Final grade (100) \_\_\_\_\_\_\_\_\_\_

Comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Grader: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date: \_\_\_\_/\_\_\_\_/\_\_\_\_\_\_\_\_

|  |  |
| --- | --- |
| 16.265 Logic Design | |
| Student Logic Number | 117 |
| Name | Erdun E |
| E-mail address (print) | Erdun\_E@student.uml.edu |
| Experiment Number | 3 |
| Date | 04/04/2018 |

|  |  |
| --- | --- |
| For grader use | |
|  |  |
| Schematic diagram submitted is different from the one in the report. (Need to re-submit the schematic diagram in the report or will be graded based on a maximum of 50 points.) | 5 points deduction |
| Cannot open file |  |
| File is not readable |  |
| Date student is notified to re-submit a schematic file by e-mail |  |
| Date schematic file received |  |

Report will be graded based on a maximum of 50 (out of 100 points) if a schematic diagram is not received within three calendar days of notification or the re-submitted schematic file still cannot be opened or is not readable.

Grade: \_\_\_\_\_\_\_\_\_\_\_Experiment 3 Design with Decoders and Multiplexers

1. Function Set Assignment

Function set number \_10\_\_

F1(x,y,z) =1 ⊕xy ⊕z

F2(x,y,z) = x ⊕y ⊕z’ ⊕xy’z

F3(w,x,y,z) =y’ (w’ + xz’) + y (w’xz’ + wx’z)

F4(w,x,y,z) =Σ m(1,4,911,13,14) + d(0,2,5,6)

F5(w,x,y,z) =(y+z)(w’+x+z)(w+y’+z’)(x’+y’+z’)

2. Design Procedures

Express all the functions in minterm list form

F1(x,y,z) = Σm (0,2,4,7)

F2(x,y,z) = Σm (0,3,6)

F3(w,x,y,z) = Σm (0,2,3,6,8,10,13)

F4(w,x,y,z) = Σm (1,4,9,11,13,14)+d(0,2,5,6)

F5(w,x,y,z) = Σm (4,6,7,8,9,10,11,13)

Design for F1 and F2

(Show the implementation of F1 and F2 by a 74155 IC and some external gates. Draw a circuit diagram.)

Design for F3

Draw the sub-function K-maps for F3 with w, x, z as expansion variables.

y

0

1

Fwxz = 001

Fwxz = 000

Fwxz = 010

Fwxz = 011

Fwxz =100

Fwxz = 101

Fwxz =110

Fwxz = 111

0

0

0

1

1

1

1

1

0

0

0

0

0

0

0

0

0

1

1

Based on the sub-function K-maps, the data inputs to the 8-to-1 multiplexers are as follows:

I0 =y’

I1 =y’

I2 =1

I3 =y’

I4 =0

I5 =y

I6 =y’

I7 =0

Design for F4 and F5

00

01

10

11

00

01

10

11

yz

wx

00

01

10

11

00

01

10

11

yz

wx

d

0

0

0

0

0

1

0

1

1

1

d

1

1

1

1

1

0

0

0

1

0

0

0

1

d

1

0

1

d

1

0

K-map for F4 K-map for F5

(i) Partition the K-maps with w and x as control signals.

00

01

10

11

00

01

11

10

yz

wx

I0

I1

I2

I3

I0

I1

I2

I3

00

01

10

11

00

01

11

10

yz

wx

0

0

0

0

0

1

0

d

1

d

1

1

1

1

1

1

0

1

0

1

0

0

0

0

1

0

1

1

1

0

d

d

F5

F4

The data inputs are as follows:

For F4 For F5

I0 = y’ I0 =y’z+yz’

I1 = y’ I1 =y’z+yz’

I2 = z I2 =z

I3 = y’z+yz’ I3 =y’z+yz’

1. Partition the K-maps with w and y as control signals.

00

01

10

11

00

01

11

10

xz

wy

I0

I1

I2

I3

00

01

10

11

00

01

11

10

xz

wy

I0

I1

I2

I3

F4

F5

0 1 0 0

1 0 1 1

1 0 1 0

0 1 0 1

d d 0 0

1 0 1 1

d 0 1 0

1 d 0 1

The data inputs are as follows:

For F4 For F5

I0 = 1 I0 =z

I1 = 0 I1 =z’

I2 = z I2 =z

I3 = x’z+xz’ I3 =x’z+xz’

(iii) Partition the K-maps with w and z as control signals.

F5

F4

00

01

10

11

00

01

11

10

xy

wz

I0

I1

I2

I3

00

01

10

11

00

01

11

10

xy

wz

I0

I1

I2

I3

0 1 0 1

1 0 0 1

1 0 1 0

0 1 0 1

d 1 0 1

d 0 0 1

d 0 1 0

1 1 0 1

The data inputs are as follows:

For F4 For F5

I0 = 1 I0 =y

I1 = y’ I1 =y’

I2 = xy I2 =xy

I3 = x’+y’ I3 =x’+y’

(iv) Partition the K-maps with x and y as control signals.

00

01

10

11

00

01

11

10

wz

xy

I0

I1

I2

I3

00

01

10

11

00

01

11

10

wz

xy

I0

I1

I2

I3

F4

F5

0 1 0 1

1 0 1 0

1 1 1 0

0 0 0 1

d d 1 d

1 0 d 0

1 1 1 0

0 0 0 1

The data inputs are as follows:

For F4 For F5

I0 = z I0 =z

I1 = wz I1 =w’z’+wz

I2 = w’+z I2 =z

I3 = z’ I3 =z’

(v) Partition the K-maps with x and z as control signals.

00

01

10

11

00

01

11

10

wy

xz

I0

I1

I2

I3

00

01

10

11

00

01

11

10

wy

xz

I0

I1

I2

I3

F4

F5

0 1 0 1

1 0 1 0

0 1 1 0

0 1 0 1

d 1 1 d

d 0 d 0

0 1 1 0

0 1 0 1

The data inputs are as follows:

For F4 For F5

I0 = 0 I0 =wy

I1 = w+y’ I1 =w+y’

I2 = w’+y I2 =y

I3 = y’ I3 =y’

(vi) Partition the K-maps with y and z as control signals.

00

01

10

11

00

01

11

10

wx

yz

I0

I1

I2

I3

00

01

10

11

00

01

11

10

wx

yz

I0

I1

I2

I3

F4

F5

0 1 1 0

0 1 1 0

0 1 1 0

0 1 0 1

d 1 d 0

1 d d 0

0 1 1 0

0 1 0 1

The data inputs are as follows:

For F4 For F5

I0 = w’ I0 =0

I1 = 1 I1 =1

I2 = x I2 =w’+x

I3 = wx’ I3 =wx’

By comparing the six different combinations for control signals, the best selection is (ii)F5 (w and y as control signals)\_\_\_\_\_\_\_\_.

3. List of ICs and unused gates

|  |  |  |  |
| --- | --- | --- | --- |
| IC number | Type number | Function | Unused gates |
| 1 | 74155 | Dual 2-to-4 decoders | None |
| 2 | 74153 | Dual 4-to-1 multiplexers | None |
| 3 | 74153 | Dual 4-to-1 multiplexers | None |
| 4 | 7400 | Quad 2-input NAND | None |
| 5 | 7400 | Quad 2-input NAND | None |
| 6 | 7402 | Quad 2-input NOR | None |
| 7 | 7420 | Dual 4-input NAND | None |
| 8 | 7486 | Quad 2-input XOR | None |

### 4. Simulation results

### Table for simulation results

(Place a check mark in the column “Incorrect results” for each simulation value that is different from the value listed in the truth table in Section 2. All don’t-care terms should have values of either 0 or 1.)

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | Simulation results | | | | | Incorrect results | | | | |
| w x y z | F1 | F2 | F3 | F4 | F5 | F1 | F2 | F3 | F4 | F5 |
| 0 0 0 0 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |  |
| 0 0 0 1 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |  |
| 0 0 1 0 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |  |
| 0 0 1 1 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |  |
| 0 1 0 0 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |  |
| 0 1 0 1 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |  |
| 0 1 1 0 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |  |
| 0 1 1 1 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |  |
| 1 0 0 0 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |  |
| 1 0 0 1 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |  |
| 1 0 1 0 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |  |
| 1 0 1 1 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |  |
| 1 1 0 0 | 1 | 0 | 1 | 0 | 0 |  |  |  |  |  |
| 1 1 0 1 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |  |
| 1 1 1 0 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |  |
| 1 1 1 1 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |  |

5. Schematic diagram

### Schematic diagram for the 4-input 5-output circuit

Attach a complete schematic diagram including the title box.

